# 40Gb/s QSFP+ Passive Copper Cable

## 40G-Q-DACx

### Product Features

- ✓ Available in lengths of 1 to 5m
- ✓ 4 independent full-duplex channels up To 11.3Gbps data rate per wavelength
- ✓ Hot-pluggable QSFP+ footprint
- ✓ RoHS compliant and Lead Free
- ✓ Power dissipation <0.1W (0~70℃)
- ✓ Commercial operating temperature optional
- ✓ Compliant with IEEE802.3ba, SFF-436

### Applications

- ✓ 40G Ethernet
- ✓ Infiniband 4X SDR DDR QDR
- ✓ 40G Telecom connections

### Product Selection

| Part Number | Lengths | Wire Size |
|---|---|---|
| 40G-Q-DAC1 | 1m | AWG30 |
| 40G-Q-DAC2 | 2m | AWG30 |
| 40G-Q-DAC3 | 3m | AWG30 |
| 40G-Q-DAC5 | 5m | AWG26 |

*For availability of additional cable lengths, please contact Fiberend.

### Regulatory Compliance

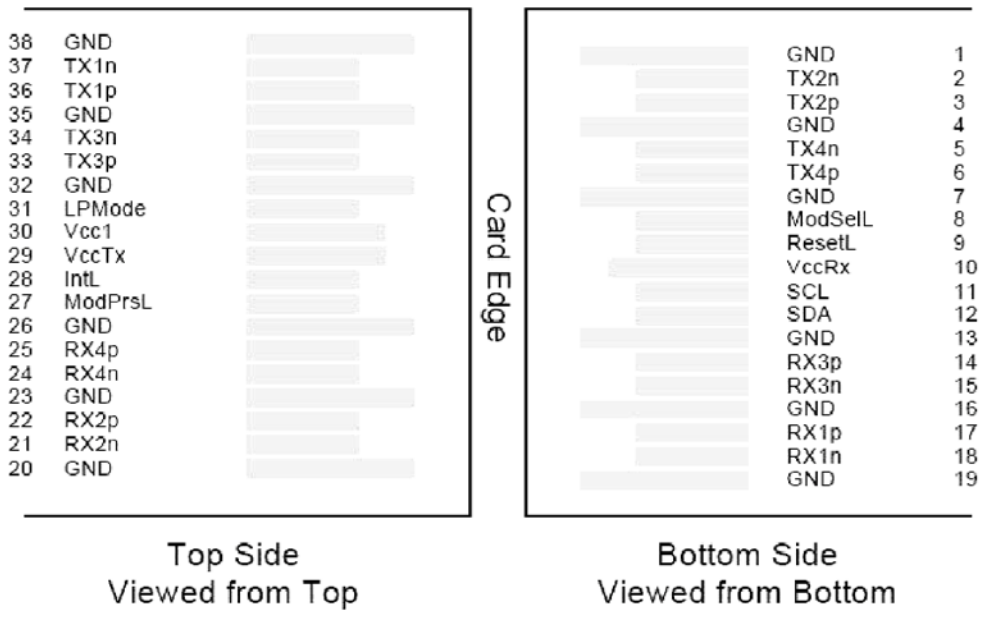
- ESD to the Electrical PINs: compatible with MIL-STD-883 Method 3015
- Immunity compatible with IEC 61000-4-3
- EMI compatible with FCC Part 15 Class B EN55022 Class B (CISPR 22B) VCCI Class B
- RoHS compliant with RoHS 2 (2011/65/EU)

### Pin Descriptions

| Pin | Symbol | Name/Description |
|---|---|---|
| 1 | GND | Ground |
| 2 | Tx2n | Transmitter Inverted Data Input, CML-I |
| 3 | Tx2p | Transmitter Non-Inverted Data output, CML-I |
| 4 | GND | Ground |

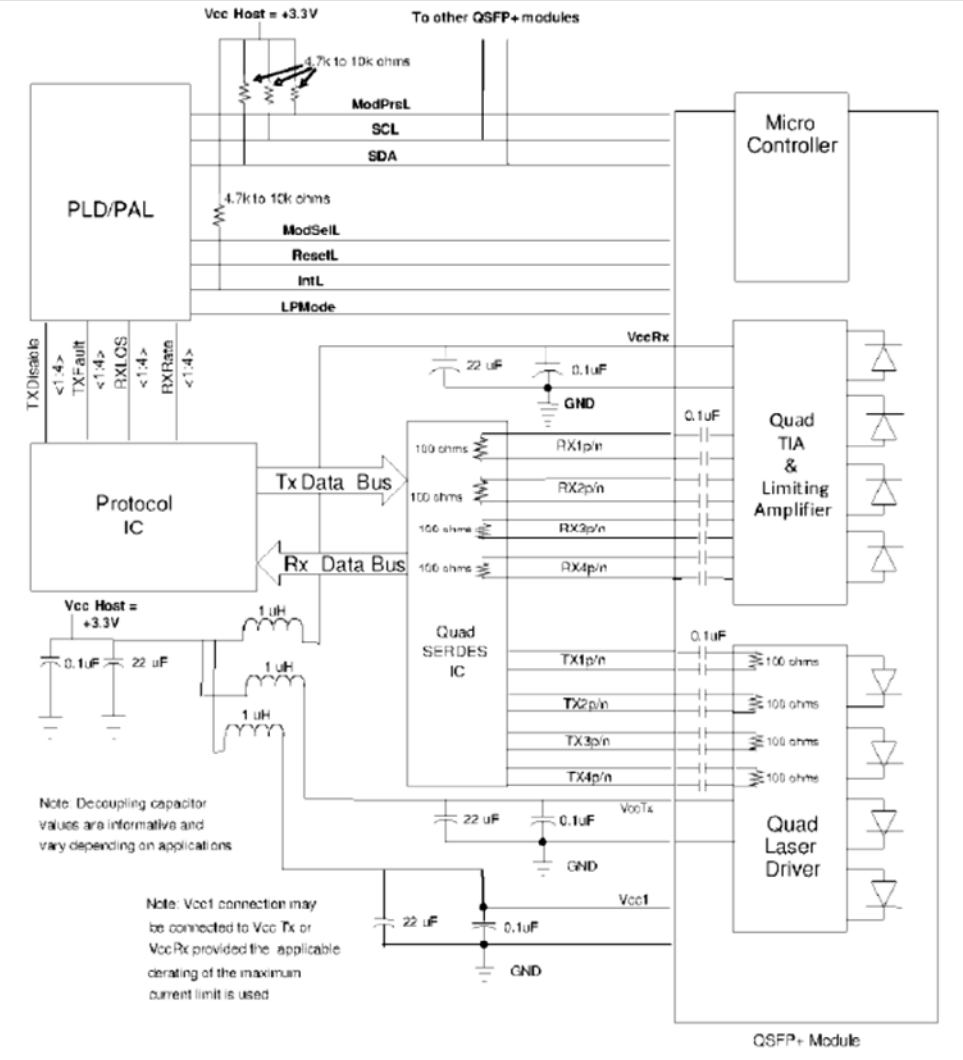
| | | |
|---|---|---|
| 5 | Tx4n | Transmitter Inverted Data Input, CML-I |
| 6 | Tx4p | Transmitter Non-Inverted Data output, CML-I |
| 7 | GND | GND |
| 8 | ModSelL | The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus. When the ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node must be biased to the “High” state in the module |
| 9 | ResetL | The ResetL pin must be pulled to Vcc in the QSFP+ module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. |
| 10 | VccRx | + 3.3V Power Supply Receiver |
| 11 | SCL | 2-Wire Serial Interface Clock |
| 12 | SDA | 2-Wire Serial Interface Data |
| 13 | GND | GND |
| 14 | Rx3p | Receiver Non-Inverted Data Output, CML-O |
| 15 | Rx3n | Receiver Inverted Data Output, CML-O |
| 16 | GND | GND |
| 17 | Rx1p | Receiver Non-Inverted Data Output, CML-O |
| 18 | Rx1n | Receiver Inverted Data Output, CML-O |
| 19 | GND | Ground |
| 20 | GND | Ground |
| 21 | Rx2n | Receiver Inverted Data Output, CML-O |
| 22 | Rx2p | Receiver Non-Inverted Data Output, CML-O |
| 23 | GND | Ground |
| 24 | Rx4n | Receiver Inverted Data Output, CML-O |
| 25 | Rx4p | Receiver Non-Inverted Data Output, CML-O |
| 26 | GND | Ground |
| 27 | ModPrsL | Module Present, connect to GND |

| | | |
|---|---|---|
| 28 | IntL | The IntL pin is an open collector output and must be pulled to host supply voltage on the host board. The INTL pin is de-asserted “High” after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of ‘0’ and the flag field is read. |
| 29 | VccTx | +3.3 V Power Supply transmitter |
| 30 | Vcc1 | +3.3 V Power Supply |
| 31 | LPMode | The LPMode pin shall be pulled up to Vcc in the QSFP+ module. This function is affected by the LPMode pin and the combination of the Power_over-ride and Power_set software control bits (Address A0h, byte 93 bits 0,1). |
| 32 | GND | Ground |
| 33 | Tx3p | Transmitter Non-Inverted Data Input, CML-I |
| 34 | Tx3n | Transmitter Inverted Data Output, CML-I |
| 35 | GND | Ground |
| 36 | Tx1p | Transmitter Non-Inverted Data Input, CML-I |
| 37 | Tx1n | Transmitter Inverted Data Output, CML-I |
| 38 | GND | Ground |




**Pin-out of Connector Block on Host Board**

## Recommend Circuit Schematic




## Absolute Maximum Ratings

| Parameter | Symbol | Min | Typ | Max | Unit | Ref. |
|---|---|---|---|---|---|---|
| Maximum Supply Voltage | Vcc | -0.5 | | +4.0 | V | |
| Storage Temperature | TS | -40 | | +85 | °C | |
| Operating Humidity | RH | 0 | | 85 | % | |

## Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit | Ref. |
|---|---|---|---|---|---|---|
| Power Supply Voltage | Vcc | 3.13 | 3.30 | 3.47 | V | |
| Power Supply Current | Icc | - | - | 0.03 | A | Commercial |
| Case Operating Temperature | Tc | 0 | - | +70 | °C | Commercial |
| Bit Rate Each Lane | Br | 1 | - | 11.3 | Gbps | |

## Electrical Characteristics (TOP=25°C, Vcc=3.3Volts)

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | |
| Input differential impedance | Rin | 80 | 100 | 120 | Ω | |
| **Receiver** | | | | | | |
| Output differential impedance | Rout | 80 | 100 | 120 | Ω | |
| **S Parameters (10GSFP+Cu Cable Assembly Specifications at B' and C')** | | | | | | |
| Differential Output/Input Reflection Coefficient | SDDxx | | | -12 + 2 × SQRT(f) | dB | 1 |
| | | | | -6.3 + 13 × log10(f/5.5) | dB | 2 |
| Common Mode Output/Input Reflection Coefficient | SCCxx | | | -7 + 1.6 ×f | dB | 3 |
| | | | | -3 | dB | 4 |

Note:

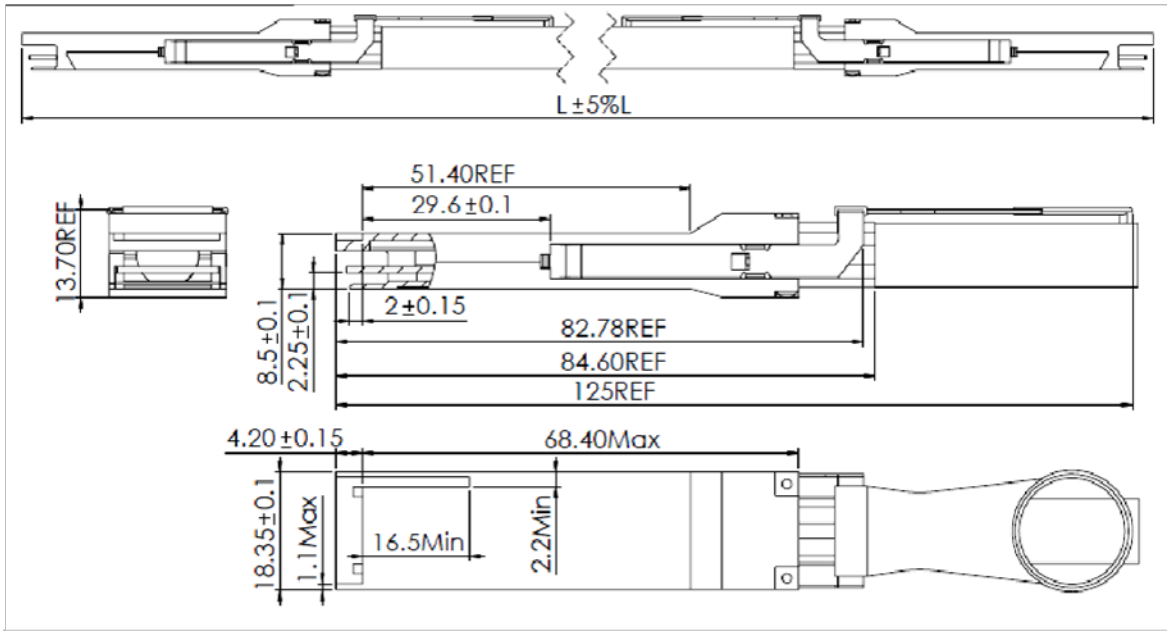
1: 0.01-4.1 GHz, reference differential impedance is 100 Ω. The dB value listed here are the same as dBe.

2: 4.1-11.1 GHz, reference differential impedance is 100 Ω. The dB value listed here are the same as dBe.

3: 0.01-2.5 GHz, reference differential impedance is 25 Ω. The dB value listed here are the same as dBe.

3: 2.5-11.1 GHz, reference differential impedance is 25 Ω. The dB value listed here are the same as dBe.

## Mechanical Specifications




**40G-Q-DACx**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Durability | | 100 | | | cycle |
| Transceiver Insert Force | | 40 | | | N |
| Transceiver Extraction Force | | 11.5 | | | N |
| Transceiver Retention Force | | 90 | | 170 | N |

## EEPROM Information

EEPROM memory map specific data field description is as below: